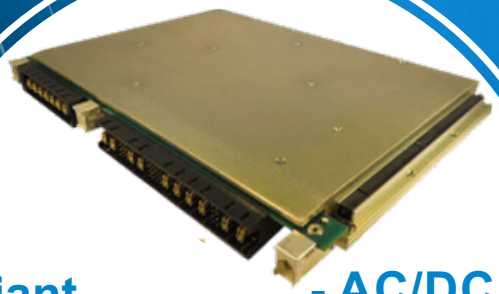
Amphenol SOCAPEX

PS SERIES
PSVA6UTPU115P1200-X
VPX AC/DC POWER SUPPLY



- Vita 62 compliant
- 6U VPX form factor
- Six outputs
- AC/DC converter
- Up to 1200W

Special Features

- VITA 62/6U
- High efficiency
- Input / Output isolation
- Remote sense
- EMI filters included
- Fixed switching frequency
- I^2C/IPMI communication
- External Inhibit & Enable
- Parallel configuration
- Indefinite short circuit protection with auto-recovery
- Over-voltage shutdown with auto-recovery
- Over temperature shutdown with auto-recovery

Electrical Specifications

AC Input
$115V_{AC} \pm 10\%$

400Hz Three-Phase

Ride-through normal transient
IAW MIL-STD-704B-F

DC Outputs (standard version)

P01*	12V/35A	Sense
P02*	12V/35A	Sense
P03	5V/12V/40A	Sense
3.3V_Aux	3.3V/15A	Sense
+12V_Aux	+12V/1A	
-12V_Aux	-12V/1A	

Total power output: 1200W

Isolation
$500V_{DC}$ Input to Output
$500V_{DC}$ Input to Case
$500V_{DC}$ Output to Case

Line/Load regulation
See Table 2 on page 6

Current Sharing
Optional for VS# Outputs
ACS or PCS

EMC
Designed to meet MIL-STD-461F CE102, CS101, CS114, CS115 & CS116.[1]

Ripple and Noise
Less than $50mV_{p-p}$, typical (max. 1%), measured across 0.1µF and 10µF on Load

Load Transient Overshoot and undershoot
Output dynamic response up to 5% at step load of 60%-90%. Output return to steady stated within 300-500µSec

Efficiency
Typical 89% (Nominal line, nominal load, room temperature)

System Management
I2C/IPMI protocol available voltages, currents and temperature for all voltages (GAx, SCL, SDA)

Power Factor for
≥ 0.87 (Full load

1. CE102 Deviation under 50KHz. Contact company for available options

*P01and P02 outputs can be connected in parallel to achieve a single 12V/70A output

Markets & Applications

Military : airborne, ground-fix, shipboard

Ruggedized, Telecom, Industrial

Protections (Thresholds and protections can be modified / removed – please consult factory).

Input

- **Inrush Current Limiter**: peak value of 5 x I_{IN} for inrush currents lasting longer than 100µs.
- **Under Voltage Lock-Out** Unit shuts down when input voltage is below 70V_{rms} ± 5V_{rms}.
- **Catastrophic Failure Protection** Fuses are available to protect from catastrophic failure. The fuses are rated not to engage due to any normal type operation.

Output

- **Active or Passive Over-Voltage Protection** Set to engage at 110%-130% of nominal voltage.
- **Overload / Short Circuit Protection** Continuous Hiccup protection (110-130%) for VS#.
  Aux Typical:
  3.3Vaux / 20A
  12Vaux. 1.5A-2A
  -12Vaux. 2.5A-3A

General

- **Over-Temperature Protection:** Shutdown at temperature of +100°C ± 5°C. Automatic recovery when temperature drops below +90°C ± 5°C. Measured at Unit edge.

Environmental

Designed to meet MIL-STD-810G and VITA 47

Temperature
Operating: –55°C to +85°C (at plug-in card edge, IAW VITA 62 CC4)
Storage: –55°C to +125°C

Altitude
810G Method 500.5, Procedure II (Operational) & VITA 47 para. 4.7 60,000 ft.

Salt Fog
Method 509.5

Humidity
810G Method 507.5 & VITA 47 Para. 4.6
Up to RH 95%

Vibration
810G Method 514.6 Procedure I Figure 514.5C-17. General minimum integrity exposure. (1 hour per axis
& VITA 47 Vibration Class V2 5-2000Hz, 0.04g^2/Hz

Shock
810G Method 516.6 Procedure I & VITA 47 Shock Class OS1
Saw-tooth, 20g peak, 11ms.

Reliability
> 314,000 hours, calculated per MIL-STD-217F Notice 2 at +65°C at wedge lock edge, Ground Fixed

Environmental Stress Screening (ESS)

Including random vibration and thermal cycles is also available. **Please consult factory for details.**

Functions and Signals (according to VITA 62.0)

Signal Name	Type	Description
FAIL*	Output	Indicates to other modules in the system that a failure has occurred in one of the outputs. Please refer to Figure 2 [1]
SYSRESET*	Output	Indicates to other modules in the system that all outputs are within their working level. Please refer to Figure 2 [1]
INHIBIT*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1 [1]
ENABLE*	Input	Controls power supply outputs. This signal in conjunction with **INHIBIT** controls the outputs. Please refer to Table 1 and Figure 1 [1]
GA0÷4*, GAP**	Input	Used for geographical addressing. GA2 is the most significant bit and GA0 is the least significant bit. [1]
SCL, SDA	Bidirectional	I2C bus Clock and Data respectively. Through this bus the voltage and temperature readouts can be shared.[1]
REF_CLK	Input	The REF_CLK signal is used to allow the power supply frequency to sync with the system frequency. [1]
VOUT SENSE	Input	The SENSE is used to achieve accurate load regulations at load terminals (this is done by connecting the pins directly to the load's terminals).
Alert Bit	Output	Indicates to other modules in the system about Input Voltage loss. Please refer to Figure 2 [1]
Active Current Share	Bidirectional	Support Active current share between Outputs. See Current Share para. [1 2 3]
PO*#_SHARE*	Bidirectional	Support Passive current share between Outputs[1]

Notes: 1. Signal referenced to **SIGNAL RTN**.

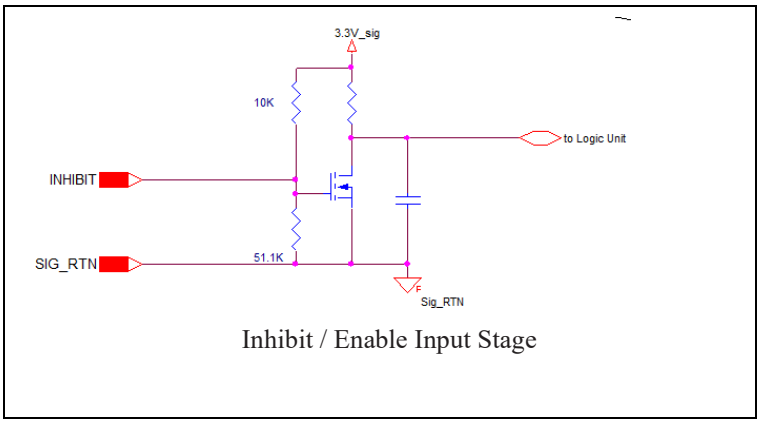
2. When not used leave open

3 In Passive or Non-Current share Current Share configuration, this pin is Internally Disconnected.

Table 1 – Inhibit and Enable Functionality

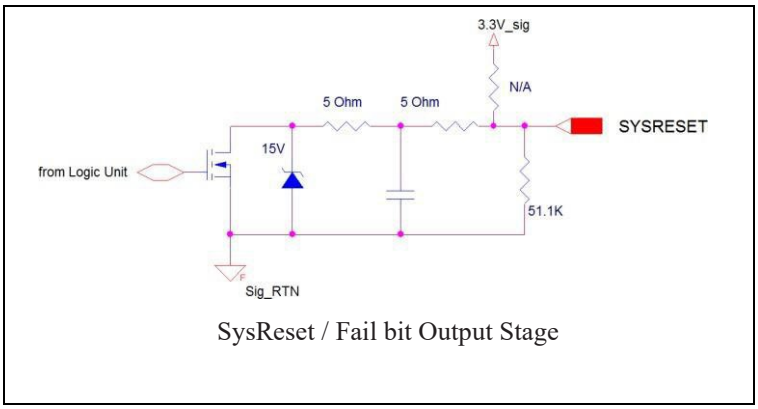
INHIBIT*	Low	Low	High	High
ENABLE*	Low	High	Low	High
VS1, VS2, VS3, ±12VAux	OFF	OFF	ON	OFF
3.3V_AUX	ON	OFF	ON	OFF

Figure 1 – Inhibit and Enable Input stage



Inhibit / Enable Input Stage

Figure 2 – SysRst and Fail Bit Output Stage



SysReset / Fail bit Output Stage

Detailed Information

1. Input Voltage Operation.

The PSVA6UTPU115P1200-X steady state operation is per Mil-STD-704. Unit will work thorough all Normal Transients per Mil-STD-704 B-F, protected to all other transients and interrupts.

2. Outputs Voltage Regulation

The PSVA6UTPU115P1200-X contains accurate internal sense lines to keep output voltage at less than 3% regulation for all Line / Load and temperature range (see Table 2).

Output	12V/25A	5V/30A	3.3V/20A	3.3VAux/5A	12VAux/1A	(-)12VAux/1A
Voltage Range	11.85 – 12.15	4.9 – 5.1	3.28 – 3.42	3.2 – 3.4	11.65 – 12.15	(-)11.85 – (-)12.15

Table 2: Outputs voltage regulation. Temperature -55°C – 85°C

2.1 Sense Lines

Sense Lines are provided for VS1, VS2 and VS3 output to compensate line voltage drop.
Sense Lines proper connection is shown in Figure 3.
Each VS# output has its own *Sense Lines*, additional common *Sense RTN Line* is provided for all VSx Outputs (VITA 62 Standard).
Contact Factory for Sense configuration different than the VITA 62 standard
Note: when two or three VS# have the same configuration (e.g. VS1 and VS2 are both 12V), sense lines of those outputs will be shorted internally.

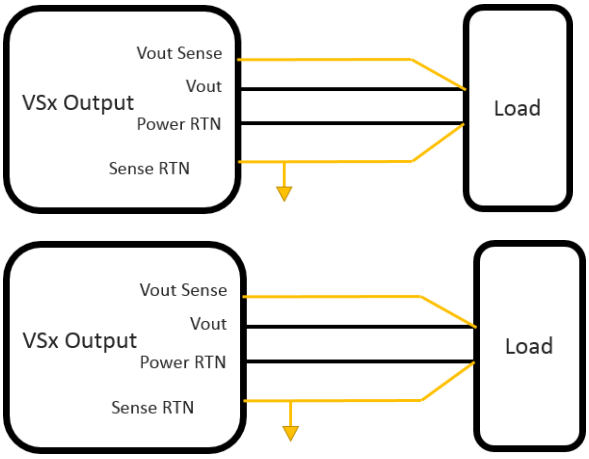


Figure 3: PSVA6UTPU115P1200-X Sense line connection

3. Current Share (C.S)

Two VS# outputs can be configured as current share to double the output current.
It is also possible to support parallel configuration of two units. VS1, VS2 and VS3 will current share with about 5-10% load balance.
All Aux Outputs can be paralleled, but would not support current sharing.
The unit can support two methods of current sharing:

3.1 Passive Current Sharing (P.C.S)

Current sharing is done in open loop, output voltage drops as a function of output load.
For Output to be P.C.S, PO#_*SHARE* Pins should be connected between two units.

3.2 Active current sharing (A.C.S)

Current sharing is done in a closed loop. All paralleled outputs are compared and feedback is used to balance their load current. The result is a more stable, less sensitive output voltage without voltage drop.

3.3 Current share connection between two Units.

3.3.1 Passive Current Share:
For a required output to P.C.S please connect the following Pins between the two units

- *PO#_Sense* & *PO#_Sense_RTN*
- *PO#_SHARE*

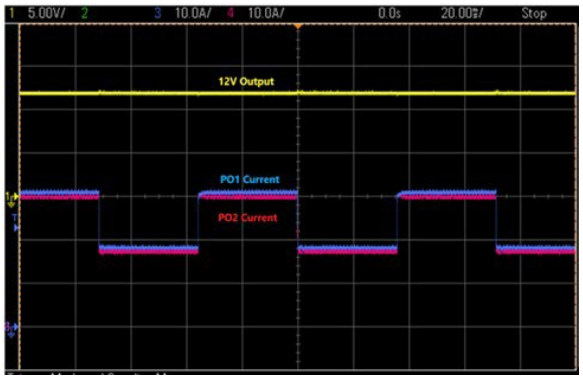
  Note: if two outputs of a unit are configured as paralleled, the Pins above are internally shorted.

3.3.2 Active Current Share:
For a required output to A.C.S please connect the following Pins between the two units

- *PO#_Sense* & *PO#_Sense_RTN*
- *PO#_SHARE*
- *PO#_ACS*

Note: if two outputs of a unit are configured as paralleled, the Pins above are internally shorted

Typical ACS Dynamic Load of Two 12V Paralleled Outputs



Note 1: When Not used, A.C.S can be left open.
When ordering P.C.S or Non-Current Share unit, those pins are Internally disconnected

4. IPMI Protocol [1]

Electrical Parameters

Vcc: 3.3VDC
Pull-up: 2.2kOhm Input capacitance: 100pf

Slave Device Addressing

- 256 address spaces
- Baud rate: 200kHz maximum
- 7 Bit Protocol
- Support Slot Addressing per VITA62
- Support Global Address 10100101 R/W

	MSB							LSB
Slot Number	A6	A5/*GAP	A4/*GA41	A3/*GA3	A2/*GA2	A1/*GA1	A0/*GA0	R/W
Slot0	1	0	0	0	0	0	0	
Slot1	1	0	0	0	0	0	1	
Slot2	1	0	0	0	0	1	0	
Slot3	1	0	0	0	0	1	1	
General Call	1	0	1	0	1	0	1	

* Slot location is determined by GAx per VITA 62.

Communication Supported

Read Command – 21Hex, deliver 64Bytes of Data. (More commands are available by request)
The communication starts when the master sends a start followed by the unit slave address, command, checksum and a stop. A second start followed by the slave address and a read will be followed by a 64 Bites response.

S	Slave Address	R/W	A	Command	A	Check sum	A	P
	A6:A0	0	0	21 Hex	0	DF Hex	0	

S	Slave Address	R/W	A	DATA	A	DATA	A	DATA	A	• • •	DATA	A	Check sum	N/A	P
	A6:A0	1	0	D7:D0	0	D7:D0	0	D7:D0	0		D7:D0	0	D7:D0	1	

Command – 21Hex read all 64 Bytes
S - Start
P- Stop

Master Transmit	Unit Transmit

Note 1 – for 46.11 Protocol, please contact factory

Memory Space

Response Byte #	Data Type	Meaning	Interpretation	Reading Range
0	U Integer, MSB First	Echo of Command		21 Hex
1	U Integer, MSB First	N/A		00 Hex
2	S Integer, MSB First	Temperature	T(C°)=+/- 7bit Dec	-55 C° to 125 C°
3	U Integer, MSB First	Reserved	00Hex	
4-5	U Integer, MSB First	VS1 Voltage	V(out) = Data/ m2	20.48V
6-7	U Integer, MSB First	VS2 Voltage	V(out) = Data/ m2	20.48V
8-9	U Integer, MSB First	VS2 Voltage	V(out) = Data/ m2	20.48V
10-11	U Integer, MSB First	3.3V Aux Voltage	V(out) = Data/ m2	20.48V
12-13	U Integer, MSB First	12V Aux Voltage	V(out) = Data/ m2	20.48V
14-15	U Integer, MSB First	(-)12V |Aux Voltage|	V(out) = Data/ m2	20.48V
16-17	U Integer, MSB First	12V VS1 Current	V(out) = Data/ m3	40A
18-19	U Integer, MSB First	3.3V VS2 Current	V(out) = Data/ m3	40A
20-21	U Integer, MSB First	5V VS2 Current	V(out) = Data/ m3	40A
22-23	U Integer, MSB First	3.3V Aux Current	V(out) = Data/ m5	20A
24-35	U Integer, MSB First	12V Aux Current	V(out) = Data/ m4	10A
26-27	U Integer, MSB First	(-)12V Aux Current	V(out) = Data/ m4	10A
28-29	U Integer, MSB First	Reserved	00Hex	
30-31	U Integer, MSB First	Reserved	00Hex	
32-51	Character String (ASCII)	Part Number	M4067-1 (Note1)	20 Characters
52-53	Decimal, MSB First	Serial Number, 2MSB Dig	X,X Dec TBD (Note2)	N/A
54-55	Decimal, MSB First	Serial Number, 2LSB Dig	X,X Dec (Note2)	N/A
56-57	Decimal, MSB First	Date Code	Week, Year (Note3)	N/A
58-59	Character String (ASCII)	Hardware Rev	B01 & B02 Boards (Note4)	2 Characters
60-61	Decimal, MSB First	Firmware Rev	X,X,X,X Dec (Note5)	4 digits
62	U Integer, MSB First	Reserved		AA Hex
63	U Integer, MSB First	Zero Checksum	Value required to make the sum of bytes 0 to 62 added to a multiple of 256	

Note:

$M_2 = 20.48/ 22^{1111}\text{-}1$

$M_3 = 40 / 22^{1111}\text{-}1$

$M_4 = 10 / 22^{1111}\text{-}1$

$M_5 = 20 / 22^{1111}\text{-}1$

Notes 1 to 5:

1. Part Number Example: PSVA6UTPU115P1200-4

Byte No'	32	33	34	35	36	37	38	39-51
Character	M	4	0	6	5	(-)	4	0
Hex	4D	34	30	36	35	2D	34	00

2. Serial Number Example: 25

Byte No'	52		53		54		55	
Dec Number	0	0	0	0	0	0	2	5
Binary	"0000"	"0000"	"0000"	"0000"	"0000"	"0000"	"0010"	"0101"

3. Date Code Example: week 35 of 2018

Byte No'	56		57	
Dec Number	3	5	1	8
Binary	"0011"	"0101"	"0001"	"1000"

4. Hardware Rev Example: B01 Rev (-), B01 Rev A

Byte No'	58	59
Character	(-)	A
Hex	2D	41

5. Firmware Rev Example: 2.1.0.0

Byte No'	60		61	
Dec Number	2	1	0	0
Binary	"0010"	"0001"	"0000"	"0000"

Pin Assignment

Connector P0

Connector type: 6450843-6 or eq.

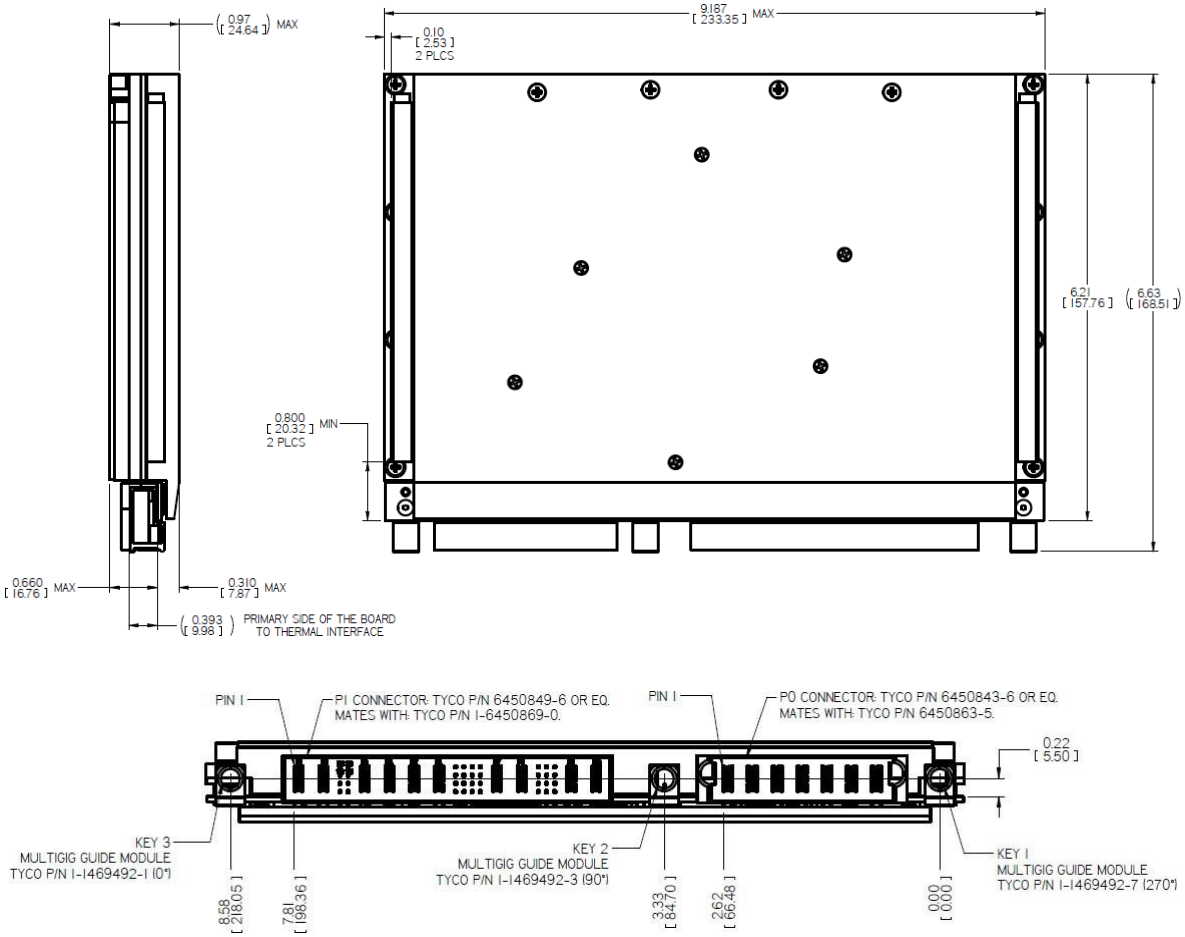
Pin Number	Signal Name
P7	PHASE A
P6	PHASE B
P5	PHASE C
P4	NEUTRAL
P3	
P2	
P1	CHASSIS_GND

Connector P1:

Connector type: 6450849-6or eq.

Pin Number	*Pin Name*
P10	12V/35A PO1
P9	12V35A PO2
A9	PO1_SENSE
B9	PO2_SENSE
C9	PO3_SENSE
D9	(-)CLK
A8	PO1_SENSE_RTN
B8	PO2_SENSE_RTN
C8	PO3_SENSE_RTN
D8	+CLK
A7	PO1_SHARE
B7	PO2_SHARE
C7	PO3_SHARE
D7	SIGNAL_RETURN
P8	POWER_RETURN
P7	POWER_RETURN
A6	+CLK
B6	-CLK
C6	-12V_AUX
D6	SYSRESET*
A5	GAP*
B5	GA4*
C5	SCL
D5	SDA
A4	GA3*
B4	GA2*
C4	GA1*
D4	GA0*
A3	VS1 ACS /N.C
B3	+12V_AUX
C3	N.C
D3	N.C
P6	5V/40A PO3
P5	5V/40A PO3
P4	POWER_RETURN
P3	POWER_RETURN
A2	N.C
B2	FAIL*
C2	INHIBIT*
D2	ENABLE*
A1	3.3Vaux Sense
B1	3.3Vaux Sense return
C1	VS3 ACS/N.C
D1	VS2 ACS/N.C
P2	3.3V/15A
P1	POWER_RETURN

Outline Drawing



Notes

1. Dimensions are in Inches [mm]
2. Tolerance is:
   .XX ± 0.01 IN
   .XXX ± 0.005 IN
3. Weight: Approx. 4 lbs

*** Specifications are subject to change without prior notice by the manufacturer.**

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